**In the Specification**

Please replace the paragraph on page 10, lines 10 through 15 with the following:

FIG. 7 shows what occurs when multiplying 8kHz and 42kHz, as at the multiplier 171 in FIG. 7. As seen in FIG. 7 [[8]], these 8kHz and 42kHz components are present in the output 172 of the multiplier 171. Also present are 50kHz and 34kHz, the sum and difference of 8kHz and 42kHz, respectively. Interfering harmonics are also present. Here, 8kHz and 42kHz were chosen to obtain an adequate separation between the harmonics and the desired frequency components.

Please replace the paragraph on page 11, lines 11 through 19 with the following:

In FIG. 8, the circuit shown in block diagram form in FIG. 6 is schematically shown in greater detail. The multipliers 171 ~~172~~ and 173 are LM 565 phase locked loops from National Semiconductor. National Semiconductor op amps LM 324 are used in the band pass filter and amplification stages 175 and 176 along with the inductor and capacitor filtering circuit elements of the values shown. The phase locked loops 181 and 182 connected as oscillators employ the LM 565 phase locked loops from National Semiconductor. $VCC_1$, from the PLL oscillator 181 at the upper right, is fed back to the multiplier 173 at the lower left and $VCC_2$ is fed back from the PLL oscillator 182 at the lower right to the multiplier 171 ~~172~~ at the upper left.